

Aditya Ajith Krishnan

[Google Scholar](#) | [Mail](#) | [GitHub](#) | [LinkedIn](#)

Summary

Doctoral student working at Knowledgeable Interactive Machines lab, with research primarily focused on cyber-physical systems and embodied AI. The aim of the work is to find mechanisms and tools to make such complex systems deterministic, safe and testable.

Education

PhD, Computer Engineering Jan 2026 – Ongoing
Arizona State University Tempe, AZ

- Advised by Prof. [Hokeun Kim](#)

MS, Computer Engineering Aug 2023 – May 2025
Arizona State University Tempe, AZ

- Computer Architecture II, Advanced Operating Systems, Real-Time Embedded Systems, Machine Learning Accelerators
- GPA: 3.3/4.0

Research Experience

Research Assistant - Knowledgeable Interactive Machines Lab, ASU – Tempe, AZ | Dec 2023- Present

- Developing a framework towards safety in Distributed Vision-Language-Action (VLA) based systems using Maxwait.
- Developing an automated cyber-physical systems testbed for 5 components using python and integration into the CI/CD pipeline of Lingua Franca open source platform.
- Developing a system with federated learning with homomorphic encryption and dynamic partial reconfiguration.
- Enhanced RTI test coverage by developing of 5 Rust RTI unit test cases for the open source project.
- Zephyr RTOS development on the nrf52dk microcontroller using the Lingua Franca framework.
- Developed a new lab experiment for Lingua Franca embedded systems lab for the real-time embedded systems course.

Graduate Services Assistant - Grader, ASU – Tempe, AZ | Aug 2024 – May 2025

- Assisted in academic evaluation for CSE 522 (Real-Time Embedded Systems) and CSE 520 (Computer Architecture) for 50+ graduate students

Publications

- **ACT: Automated CPS Testing for Open-Source Robotic Platforms** (2026): Proceedings of the 7th ACM/IEEE International Conference on Automation of Software Test (AST 2026), April 13 - 14, 2026.
- **Towards Efficient Privacy-Preserving Federated Learning on Edge with Reconfigurable FPGA** (2025): in Proceedings of the 28th Forum on specification and Design Languages (FDL 2025), September 10 - 12, 2025.

Industry Experience

Embedded Software Engineer, VVDN Technologies – Kochi, India | Aug 2020 – Jul 2022

Project: Hardware acceleration of the AMD U25N SmartNIC

- Ported and optimized driver modules for U25N SmartNIC, improving platform stability and **L2/L3 throughput by 22% using OVS** in high-performance workloads (**VxLAN, L2GRE, and VM-to-VM switching**)
- Engineered and validated the SmartNIC's 3 most critical features — **Switching, ConnTrack, and DPR** modules.
- Architected a Dynamic Partial Reconfiguration (DPR) driver and application module from scratch; **reduced FPGA reconfig time by 66%** enabling faster deployment and function exchange.
- Delivered driver support for **5 critical firmware components** (reset, mode control, flash select, statistics, card ID).
- Led the driver release and validation phase; **coordinated with the FPGA and QA teams** to resolve integration issues.

Academic Projects

- **Deep Learning Performance Profiling** (2025): **Profiled MLP, CNN, and BERT** models on NVIDIA 3060 using Nsight Systems and Compute, measuring GPU utilization, DRAM bandwidth, and power draw.
- **Features on xv6 Operating System** (2024): Implemented 4 features on the xv6 operating system: Scheduling algorithms, bootloader, trap and emulate of VM, fork functionality, and process creation.
- **Bringup of Agilex 7 SoC FPGA Dev Kit** (2024): Bootstrapped HPS-first mode on Arm Cortex-A53 with Yocto images and benchmarked ResNet across 7 architectures using Intel FPGA AI Suite.